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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Total Number of Pages in This Submission: 47

Application Number	09/805,395
Filing Date	3/13/2001
First Named Inventor	Harold Hansen II
Art Unit	2645
Examiner Name	Ming Chow
Attorney Docket Number	16312-P001C1X1

ENCLOSURES *(Check all that apply)*

- [x] Fee Transmittal Form
  - [x] Fee Attached
- [ ] Amendment/Reply
  - [ ] After Final
  - [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
- [ ] Certified Copy of Priority Document(s)
- [ ] Reply to Missing Parts/ Incomplete Application
  - [ ] Reply to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Drawing(s)
- [ ] Licensing-related Papers
- [ ] Petition
- [ ] Petition to Convert to a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
- [ ] Terminal Disclaimer
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- [ ] CD, Number of CD(s) _____
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- [ ] After Allowance Communication to TC
- [ ] Appeal Communication to Board of Appeals and Interferences
- [x] Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
- [ ] Proprietary Information
- [ ] Status Letter
- [x] Other Enclosure(s) (please Identify below):

2 references; Return Postcard

Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	Winstead Sechrest & Minick P.C.		
Signature			
Printed name	Kelly K. Kordzik		
Date	2/28/2005	Reg. No.	36,571

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PTO/SB/17 (11-04)
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Effective on 10/01/2004. Patent fees are subject to annual revision.

FEE TRANSMITTAL
For FY 2005

☑ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) **250.00**

Complete if Known	
Application Number	09/805,395
Filing Date	3/13/2001
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FEE CALCULATION

1. BASIC FILING FEE

Fee Description	Fee ($)	Small Entity Fee ($)	Fee Paid($)
Utility Filing Fee	790	395	
Design Filing Fee	350	175	
Plant Filing Fee	550	275	
Reissue Filing Fee	790	395	
Provisional Filing Fee	160	80	

Subtotal (1) $ _____

FEE CALCULATION (continued)

2. EXTRA CLAIM FEES

Fee Description	Fee ($)	Small Entity Fee ($)
Each claim over 20	50	25
Each independent claim over 3	200	100
Multiple dependent claims	360	180
For Reissues, each claim over 20 and more than in the original patent	50	25
For Reissues, each independent claim more than in the original patent	200	100

Total Claims	Extra Claims	Fee ($)	Fee Paid ($)
_____ - 20 or HP =	_____	x _____	= _____

HP = highest number of total claims paid for, if greater than 20

Indep. Claims	Extra Claims	Fee ($)	Fee Paid ($)
_____ - 3 or HP =	_____	x _____	= _____

HP = highest number of independent claims paid for, if greater than 3

Multiple Dependent Claims	Fee ($)	Fee Paid ($)
	_____	_____

Subtotal (2) $ _____

3. OTHER FEES

Fee Description	Fee ($)	Small Entity Fee ($)	Fee Paid($)
1-month extension of time	120	60	
2-month extension of time	450	225	
3-month extension of time	1,020	510	
4-month extension of time	1,590	795	
5-month extension of time	2,160	1,080	
Information disclosure stmt. fee	180	180	
37 CFR 1.17(q) processing fee	50	50	
Non-English specification	130	130	
Notice of Appeal	500	250	
Filing a brief in support of appeal	500	250	250.00
Request for oral hearing	1,000	500	
Other: _____			

Subtotal (3) $ 250.00

SUBMITTED BY

Signature		Registration No. (Attorney/Agent) 36.571	Telephone 512.370.2851
Name (Print/Type)	Kelly K. Kordzik		Date 2/28/2005

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application: Hansen et al.

Serial No.: 09/805,395

Filed: March 13, 2001

Art Unit: 2645

Examiner: Ming Chow

For: TELEPHONE CALL/VOICE PROCESSING SYSTEM

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF

I. REAL PARTY-IN-INTEREST

The real party in interest is Estech Systems, Inc., who is the assignee of the entire right and interest in the present Application.

CERTIFICATION UNDER 37 C.F.R. § 1.8

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Toni Stanley
Signature
Toni Stanley
(Printed name of person certifying)

II. RELATED APPEALS AND INTERFERENCES

There are no appeals or interferences known to Appellants, the Appellants' legal representative, or assignee which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 1-3, 6, 12, 18-20, 24-27, 58-61 and 69-84 are pending in the Application, and also stand rejected.

IV. STATUS OF AMENDMENTS

There were no amendments to the claims filed after the final rejection. However, an amendment to the Specification has been recently filed on February 9, 2005 in order to list a priority to a provisional patent application.

V. SUMMARY OF THE INVENTION

The present invention is a telephone and voice mail system 100 requiring only a single processing means 101 for controlling operations of both the telephone system and the voice mail system. (Fig. 1) The single processing means 101 communicates with a hard disk 107, which stores programs for running the various operations of this system, voice prompts and all voice mail messages. (Page 9, line 15 - page 10, line 6) The single processing means 101 is coupled to a signal processing circuitry 102, which emulates analog electronics that would be used for filters, tone decoder, and generators, etc. The single processing means 101 and signal processing circuitry 102 are coupled 122 to CO lines (Fig. 3) and station lines (Fig. 3) by a digital cross-point

matrix 103, which can connect any voice path (also referred to herein as a "call") to another voice path. (Page 12, lines 3-13)

A record sequence activation signal may be transmitted from EKT 1400 to interface 306 via transformer 1102 (see Fig. 11), which passes the signal to microprocessor 101 through data transceiver and multiplexer 302 and microcontroller 301. Next, in step 402, a determination is made whether or not EKT 1400 is connected to a valid call. (See Fig. 4) A valid call is defined as energy being detected on the line, and the energy is not dial tone. If not, the process proceeds to step 403 to ignore the record activation signal. However, if EKT 1400 is connected to a valid call, the process proceeds to step 404 to determine whether or not a record resource is available. This may be accomplished by determining whether or not a recording buffer 1003 is available in DSP 102. If not, the process proceeds to step 405 to display an error message to the telephone extension user. This may be accomplished by some type of visual (e.g., on display 1401 or via an LED on EKT 1400) or audible indication provided EKT 1400.

VI. REJECTIONS

1. Claim 71 stands rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in a specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

2. Claims 1-3, 12, 18-20, 24-27, 71-73 and 84 stand rejected under 35 U.S.C. § 102(e) as being anticipated by *Heidari* (U.S. Patent No. 5,790,957).

3. Claims 74 and 77 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Heidari* as applied to claim 1, and in view of *Smith* (U.S. Patent No. 6,597,924).

4. Claims 6, 58-61, 69, 75-76, 79 and 81-82 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Heidari* and in view of *Alfred* (U.S. Patent No. 6,393,275).

5. Claims 78 and 80 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Heidari* as applied to claim 1, and in view of *Alfred* and *Smith* (U.S. Patent No. 6,597,924).

6. Claim 83 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over *Heidari* as applied to claim 1, and in view of *Alfred* and *Smith*.

VII. ARGUMENTS

1. Claim 71 is not properly rejected under 35 U.S.C. § 112, first paragraph.

Specifically, the Examiner asserts that the phrase "the plurality of telecommunications devices connected to the system as telephone extensions accessible solely through the switching circuitry" is not disclosed by the Specification. The Examiner goes on to further assert that since the Specification discloses a DSP for call signal processing but the DSP does not perform a switching function, then call signals must be processed by the DSP to reach the extensions, and therefore the extensions are not accessible solely through the switching circuitry. Applicants respectfully traverse these assertions by the Examiner.

For a claim limitation to be supported by the Specification, one must be able to read that claim limitation onto the Specification. Since the Specification and the drawings clearly show that the telephone extensions are connected to the system solely through the switching circuitry, this claim limitation is fully supported. Note that the telephone extensions are not part of the telephone call and voice processing system. The telephone extensions are connected to the telephone call and voice

processing system by only one means, and that is the switching circuitry. Thus, the rest of the telephone call and voice processing system 100 must go through the switching circuitry to be able to access the telephone extensions (see Fig. 14). The DSP is part of the system 100. How does the DSP access the telephone extensions? Solely through the switching circuitry. The same with every other portion of the system 100. The claim does not recite that the telephone extensions are accessible by something other than the system solely through the switching circuitry. Instead, the claim phrase merely recites that these telecommunications devices, i.e., telephone extensions, are connected to the system 100 solely through the switching circuitry 103. One skilled in the art would easily be able to make and use the present invention as recited within claim 71 through the use of the Specification.

2. Claims 1-3, 12, 18-20, 24-27 and 70-73 and 84 are not properly rejected under 35 U.S.C. 102(e) as being anticipated by *Heidari*.

A. Claims 1, 12, 27

With respect to claims 1, 12 and 27, the Examiner is equating the plurality of telecommunications devices recited in the claims with the speaker 14, digital receive circuit 44 and analog receive circuit 46 of Fig. 1 in *Heidari*. Applicants respectfully traverse such an assertion by the Examiner in that these are not telecommunications devices, and that the Examiner is interpreting this claim language in an unreasonably broad manner. The Examiner may interpret the claims with their broadest reasonable meaning of the words, but this broad interpretation must still be limited to the ordinary usage of such terms as they would be understood by one of ordinary skill in the art, taking into account whatever enlightenment by way of definitions or otherwise that may be afforded by the written description contained in Applicants' Specification. MPEP § 2111. The broadest reasonable interpretation of the claims must also be consistent with the interpretation that those skilled in the art would reach. *Id.* Nevertheless, in order to move the Application towards allowance, Applicants previously amended claims 1, 12 and 27 so that two or more of the

plurality of telecommunications devices each further comprises both a speaker and a microphone for enabling a user to audibly communicate with the call. None of the speaker 14, digital receive 44, or analog receive 46 is a telecommunications device that further comprises both a speaker and a microphone for enabling a user to audibly communicate with the call. Though the cellular telephone 10 disclosed in *Heidari* has a microphone and a speaker, there is no capability within *Heidari* for the switching circuitry (as asserted by the Examiner) within telephone 10 to connect an incoming call to one of a plurality of telecommunications devices, wherein two or more of such devices each have both a microphone and a speaker permitting a user to communicate with the call. As a result, claims 1, 12 and 27, and all claims depending therefrom, are not anticipated by *Heidari*.

In paragraph 3, page 4 of the final rejection dated October 5, 2004, and in paragraph 3, pages 3-4 of the Advisory Action, the Examiner attempts to address Applicants' foregoing arguments, but does so in such a confusing way there is really no logic to the Examiner's assertions. The only way to make sense out of what the Examiner is attempting to assert is to redirect the Examiner's attention to the claims as a whole and how the Examiner attempts to read the claim limitations onto *Heidari*. The claims recite switching circuitry. In one instance, the Examiner asserts that such switching circuitry is item 60 in Fig. 1 of *Heidari*. Switch 60 is implemented within a cellular telephone 10. Telephone 10 is operable for operating in either a digital mode or an analog mode. Column 1, lines 5-9. Switch 60 is included in the DSP 26 to enable selection of the analog or digital mode of communication. Column 4, lines 46-48. The Examiner first attempts to map the recited telecommunication devices to digital receive 44 and analog receive 46 in *Heidari*. The Examiner then goes onto assert that switch 60 connects a received call to either the digital receive 44 or the analog receive 46, based on the information accompanying the call that the call is either an analog call or a digital call. This is incorrect. Switch 60 connects either the digital receive 44 or the analog receive 46 to the speaker 14 through the codec 24. Column 7, lines 7-9. The incoming call is not connected to either 44 or 46 by

switch 60 as a function of whether the received call is analog or digital. See column 6, lines 24-35. The Examiner next attempts to assert that switch 60 connects the call to the speaker 14 based on the information accompanying the call that the call is an incoming call and the recipient is available. First, the Examiner has no objective support for this assertion that switch 60 operates in this manner. Second, *Heidari* does not teach such a reasoning for how switch 60 operates, and as Applicants have asserted above, operates under a different manner whereby switch 60 is operable to connect the digital receive 44 or the analog receive 46 to the speaker 14 depending upon the type of call received by antenna 52 of cell phone 10.

Next, neither speaker 14, digital receive 44, or analog receive 46 are a telecommunications device that comprises both a speaker and a microphone for enabling a user to audibly communicate with the received call.

The Examiner then goes on to assert that switches 84 and 86 could be the switching circuitry recited in the claims, and that such switching circuitry connects the memory in accordance with information accompanying the call that the call is either inputting or outputting data from the memory. Again, the Examiner has no objective support for such an assertion. Secondly, such an assertion by the Examiner does not address the claim language. Further, memory 76 is not a telecommunications device that comprises both a speaker and a microphone for enabling a user to audibly communicate with the received call.

The bottom line here is that the Examiner is unreasonably interpreting the teachings of the prior art to attempt to compare *Heidari* to the claimed invention. This is not permitted.

B. Claims 3, 70

Regarding claims 3 and 70, which recite a "digital crosspoint matrix," the Examiner is making an unreasonably broad interpretation of this term in asserting that Items 60, 64, 66, and 68 within Fig. 1 of *Heidari* teach such circuitry. The Examiner

is respectfully requested to refer to page 142 of *Introduction to Telephones and Telephone Systems*, by A. Michael Noll, Third Edition. (Applicants attach hereto a page from this book noting that it has a copyright of 1998, with this version being the third edition, which is a revised edition of the second edition having a copyright of 1991.) (Moreover, despite the date of this reference, it is still dispositive of the well-known meaning of this term, which the Examiner has failed to adequately rebut.) Fig. 6.12 clearly differentiates between a rotary switch (a), an on-off switch (b), and a matrix switch (c). Switches 60 and 64 in *Heidari* are on-off switches, while switches 66 and 68 are rotary switches. As page 142 of the reference clearly shows, these are different than matrix switches (c), and one skilled in the art would understand such a difference. It is preposterous to equate the recited digital crosspoint matrix to the individual switches shown in *Heidari*. Again, the Examiner is simply making unreasonable interpretations of the prior art, which is not allowed. MPEP § 2111. Further, the Examiner asserts that Newton's Telecom Dictionary defines "crosspoint" as "a single element in an array of elements that comprise a switch." Items 60, 64, 66 and 68 are not single elements in an array of elements that comprise a switch. Each is an individual rotary switch. One skilled in the art would not equate the switches shown in *Heidari* as a digital crosspoint matrix. Those items in *Heidari* do not meet the definition of "digital crosspoint matrix."

Further, an example of a digital crosspoint switch is provide in the Specification as part no. 8980 available from MITEL. Page 12, lines 5-7. MITEL was renamed as Zarlink in 2001. A data sheet for the 8980 is attached, showing clearly that the switches in *Heidari* are not to be equated with a digital crosspoint switch.

C. Claim 20

With respect to claim 20, the Examiner still has not addressed Applicants' traversals. Applicants have previously asserted that the vocoder 70 in *Heidari* is not capable of recording all or a portion of an incoming call during an off-hook state.

This is still the case. Vocoder 70 is merely comprised of compression and expansion circuits. The vocoder 70 does not meet the claim limitations.

D. Claim 71

With respect to claim 71, as noted above, the language in claim 71 was merely moved, not newly added. Therefore, Applicants were entirely correct in asserting that the Examiner had failed to address these claim limitations in the previous Office Actions. The Examiner has now merely referred to all of Fig. 1 in *Heidari* as showing that *Heidari* teaches "the plurality of telecommunications devices connected to the system as telephone extensions accessible solely through the switching circuitry." This is an insufficient rejection, since it does not point out where such plurality of telecommunications devices connected as telephone extensions solely through the switching circuitry is shown in Fig. 1. There are no plurality of telephone extensions shown in Fig. 1. It is unreasonable for the Examiner to assert that any of the items shown in Fig. 1 of *Heidari* are telephone extensions. One skilled in the art would not refer to anything shown in Fig. 1 of *Heidari* as a telephone extension. The Examiner must review the claims and interpret the prior art in a reasonable manner.

Furthermore, on page 9 of Paper No. 14 and page 8 of the Final Rejection, the Examiner admits that *Heidari* fails to teach such telephone extensions, and thus by the Examiner's own admission, *Heidari* cannot anticipate claim 71.

Yet still further, the telecommunications devices cited in *Heidari* by the Examiner as speaker 14, and circuits 44 and 46 are clearly not telephone extensions. A telephone extension is known in the art as an additional telephone connected to a line. Newton's Telecom Dictionary, 17th Edition, page 264.

The Examiner further asserts that the caller and the callee must be a plurality of telephone extensions. However, this does not address the claim language. The claims recite that the plurality of telecommunications devices are the telephone

extensions. The Examiner has not asserted that the caller and the callee are telecommunications devices.

E. Claim 72

With respect to claim 72, the Examiner has asserted on page 6 of the final rejection that all of the rejections as stated in claims 1 and 18 previously supplied apply to the rejection of claim 72. Under such a rationale, for the Examiner's § 103 rejection of claim 72 to be valid, it would mean that all of the claim limitations recited in claim 72 already existed in claims 1 and 18, and thus the rejection of those claims by the Examiner would apply. The problem with such an assertion by the Examiner is that there is a limitation within claim 72 not found within either of claims 1 or 18. Claim 72 recites "circuitry for permitting a user of a telephone coupled to the system to monitor a voice mail message while the message is being recorded into the user's mailbox." Claims 1 and 18 do not recite this claim limitation. Therefore, the Examiner's rejections of claims 1 and 18 cannot validly reject claim 72, since the Examiner has not shown a *prima facie* case of anticipation in rejecting claim 72.

Furthermore, *Heidari* does not in any way teach or suggest circuitry for permitting a user of a telephone coupled to the system to monitor a voicemail message while the message is being recorded into the user's mailbox. Column 1, lines 63-66 of *Heidari* refers to the recording of a call while the person utilizing the telephone is able to maintain a conversation. This is not the same as monitoring a voicemail message while the message is being recorded into the user's mailbox.

F. Claim 73

Claim 73 is dependent upon claim 1. Claim 73 recites that the information recited in claim 1 is detected DTMF tones. Therefore, reading claims 1 and 73 together, they would recite that "the switching circuitry connects the call to one of a plurality of telecommunications devices coupled to the system in accordance with

detected DTMF tones accompanying the call that identifies the telecommunications device . . ." In rejecting claim 1, the Examiner has asserted that the telecommunications devices recited within the claims are represented by the microphone 12, the speaker 14, the digital receive circuitry 44, or the analog receive circuitry 46. Applicants assert that *Heidari* does not teach or suggest that a received call is switched to any of these devices in accordance with DTMF tones. In the Advisory Action, the Examiner asserts that the "information accompanying a call" must be the DTMF tone. Applicants traverse this assertion by the Examiner. The Examiner has not supported such an assertion with any objective evidence. The Examiner cannot support his assertion based on an assumption.

G. Claim 84.

Claim 84 is dependent upon claim 1 and further recites that each of the two or more of the plurality of telecommunications devices are separately operable telephone extensions. The Examiner attempts to assert that everything shown in Fig. 1 of *Heidari* is a telecommunications device. Applicants disagree. Nothing shown in Fig. 1 of *Heidari* is a separately operable telephone extension, as that term is well known in the art, especially items 12, 14, 44, and 46. Such an assertion by the Examiner is without any reasonable objective basis. See MPEP § 2111.

3. Claims 74 and 77 are not properly rejected under 35 U.S.C. § 103 as being unpatentable over *Heidari* in view of *Smith* (U.S. Patent No. 6,597,924).

A. Claim 74

Claim 74 depends upon amended claim 1, and is patentable for similar reasons as given above with respect to claim 1.

B. Claim 77

With respect to claim 77, on page 9 of Paper No. 14, the Examiner has admitted that *Heidari* fails to teach that the switching circuitry connects the incoming call to a plurality of telephone extensions. Thus, the Examiner has admitted that

Heidari fails to disclose this claim limitation, and the Examiner is relying upon *Heidari* to teach such claim limitations. Further, the combination of *Heidari* and *Smith* fails to teach such claim limitations. Applicants further incorporate their arguments from above with respect to claim 71.

Smith teaches a cellular telephone 16 coupled to a CO trunk in Figs. 1 and 2. Combining *Smith* and *Heidari*, there still is no teaching or suggestion of switching circuitry that connects an incoming call to one of a plurality of telecommunication devices coupled to the system as telephone extensions to the system. As asserted above, the "devices" noted by the Examiner in *Heidari* are not telephone extensions, as this term is known in the art. Plus, on page 9 of Paper No. 14, the Examiner admitted as much.

4. Claims 6, 58-61, 69, 75-76, 79 and 81-82 are not properly rejected under 35 U.S.C. § 103 as being unpatentable over *Heidari* in view of *Alfred* (U.S. Patent No. 6,393,275).

A. Claims 6, 58, 69 and 81

The Examiner admits that *Heidari* fails to teach the switching circuitry connecting the incoming call to a telecommunications device coupled to the system from among a plurality of telecommunications devices connected as telephone extensions. The Examiner attempts to overcome this deficiency by referring to the Abstract and column 1, lines 40-52 of *Alfred*. However, what *Alfred* is teaching is the connection by a base station of a call to a plurality of cell phones communicating with the base station. As taught in *Alfred* at column 5, lines 25-35, the modified mobile switching center 100, or base station, performs all of the switching of incoming calls to cellular telephones 112, 114, 122. According to the Examiner's interpretation of *Heidari*, *Heidari* teaches switching occurring within the cell phone to various ones of circuits 14, 44, 46. However, the switches the Examiner has cited to in *Heidari* are not capable of switching an incoming call to a plurality of cellular telephones, or extensions. The switching of incoming calls in a base station to a plurality of cellular

telephones communicating with the base station combined with the switches 58, 60, 84, 86, 68, 66 in *Heidari* switching signals to the analog receive circuit 46, digital receive circuit 44, or speaker 14 does not lead one skilled in the art at the time the invention was made to a telephone call and processing system that switches incoming calls to one of a plurality of telephone extensions where the system also includes voice processing circuitry for automatically interacting with the call where such switching circuitry and voice processing circuitry are controlled by a single processing means and by a single set of software that controls both of the switching circuitry and the voice processing circuitry. *Alfred* does not teach, contrary to the Examiner's assertion, that one of the cellular phones serves as the parent while the others serve as extensions of that parent. Instead, the processes disclosed in the Specification of *Alfred* and described in the flow diagrams are all accomplished within the base station, or MMSC. Though one of the telephones may be "designated" as a parent, switching does not occur within that telephone, but instead remains with the MMSC. In fact, it could be said that the *Heidari* cellular telephone would be merely one of the telephones 112, 114, 122 within the *Alfred* system. In such a case, it would be clear that the switching circuitry and voice processing circuitry would not be controlled by a single set of software with a single processing means.

B. Claims 61, 81

Regarding claim 61, the Examiner has failed to specifically address these claim limitations. Moreover, regarding claim 81, nothing in the cited art, and especially *Heidari* identifies any of the "devices" cited by the Examiner so that a call is switched to it.

In response in the Advisory Action, all the Examiner has done is to assert that the modified system of *Heidari* in view of *Alfred* meets the claimed "switching circuitry connects incoming call to a telecommunications device (of *Heidari* from among a plurality of telecommunication devices extensions of *Alfred*), and that the

telephone extensions taught by *Alfred* serve as calling parties and the telephone taught by *Heidari* serves as the called party." The problem with this response by the Examiner is that it does not address all of Applicants' traversals on pages 17 and 18 of their previous response. Again, the Examiner is respectfully requested to refer to MPEP § 707.07(f). The Examiner must respond to all traversals by Applicants.

5. Claims 78 and 80 are not properly rejected under 35 U.S.C. § 103 as being unpatentable over *Heidari* in view of *Alfred* and *Smith*. These claims are patentable because they depend upon allowable claims.

6. Claim 83 is not properly rejected under 35 U.S.C. § 103 as being unpatentable over *Heidari* as applied to claim 1 and in view of *Alfred* and *Smith*.

Applicants arguments given above with respect to claims 1 and 6 are incorporated herein. Further, the Examiner is relying solely upon hindsight reasoning to combine the three prior art references. Nothing within *Smith* or *Alfred* teaches or suggests that the switching circuitry can be combined with the voice processing circuitry in the cellular telephone of *Heidari*. The switching circuitry cited by the Examiner in *Heidari* is not in any way similar to the switching circuitry recited in *Smith* and *Alfred*. One skilled in the art at the time the invention was made would not have combined these three prior art references to arrive at claim 83. The motivation provided by the Examiner on page 11 of the Office Action is the Examiner's subjective opinion, which does not amount to objective evidence required to support a *prima facie* case of obviousness.

Further, the "devices" in *Heidari* cited by the Examiner do not have a voice mail box associated with any of them.

Respectfully submitted,

WINSTEAD SECHREST & MINICK P.C.

Attorneys for Appellants

By: _____
Kelly K. Kordzik
Reg. No. 36,571

P.O. Box 50784
400 North Ervay Street
Dallas, Texas 75201
(512) 370-2851

APPENDIX

1. A telephone call and voice processing system comprising:

switching circuitry for receiving a call, wherein the switching circuitry connects the call to one of a plurality of telecommunications devices coupled to the system in accordance with information accompanying the call that identifies the telecommunications device, wherein two or more of the plurality of telecommunications devices each further comprises both a speaker and a microphone for enabling a user to audibly communicate with the call; and

voice processing circuitry for automatically interacting with the call, wherein the switching circuitry and the voice processing circuitry are controlled by not more than one microprocessor.

2. The system as recited in claim 1, wherein the voice processing circuitry further comprises a signal processing circuitry coupled to the one microprocessor.

3. A telephone call and voice processing system comprising:

switching circuitry for receiving a call, wherein the switching circuitry connects the call to a telecommunications device coupled to the system; and

voice processing circuitry for automatically interacting with the call, wherein the switching circuitry and the voice processing circuitry are controlled by a single processing means, wherein the voice processing circuitry further comprises a signal processing circuitry coupled to the single processing means, wherein the switching circuitry further comprises a digital cross-point matrix coupled to the single processing means and to the signal processing circuitry.

6. A telephone call and voice processing system comprising:

a plurality of telecommunications devices coupled to the system as extensions;

switching circuitry for receiving a call, wherein the switching circuitry connects the call to one of the telecommunications devices; and

voice processing circuitry for automatically interacting with the call, wherein the switching circuitry and the voice processing circuitry are controlled by a single processing means, wherein the single processing means is controlled by a single set of software operable for controlling both the switching circuitry and the voice processing circuitry.

12. A telephone call and voice processing system comprising:

switching circuitry for receiving a call, wherein the switching circuitry connects the call to a telecommunications device coupled to the system, wherein two or more of the plurality of telecommunications devices each further comprises both a speaker and a microphone for enabling a user to audibly communicate with the call; and

voice processing circuitry for automatically interacting with the call, wherein the switching circuitry and the voice processing circuitry are controlled by a single processing means, wherein the voice processing circuitry further comprises a signal processing circuitry coupled to the single processing means, wherein the signal processing circuitry further includes:

a DTMF receiver operable for recognizing DTMF tones from the call and instructing the switching circuitry to connect the call to the telecommunications device identified by the DTMF tones.

18. The system as recited in claim 2, further comprising circuitry operable for recording all or a portion of the call during an off-hook state after the telecommunications device is connected to the call.

19. The system as recited in claim 18, wherein the recording circuitry operates in response to a user manually pressing a button on a telephone set.

20. A telephone call and voice processing system comprising:

switching circuitry for receiving a call, wherein the switching circuitry connects the call to one of a plurality of telecommunications devices coupled to the system in accordance with information accompanying the call that identifies the telecommunications device;

voice processing circuitry for automatically interacting with the call, wherein the switching circuitry and the voice processing circuitry are controlled by not more than one microprocessor; and

circuitry operable for recording all or a portion of the call during an off-hook state after the telecommunications device is connected to the call, wherein the recording circuitry operates in response to a user manually pressing a button on a telephone set, and wherein the recording circuitry further comprises:

circuitry for coupling a recording buffer in signal processing circuitry to the call, wherein the signal processing circuitry is coupled to the one processor.

24. The system as recited in claim 1, further comprising:

circuitry for listening to a voice signal at a telephone extension coupled to the system;

circuitry for activating a recording sequence to record the voice signal; and

circuitry for storing the recorded voice signal in a digital memory.

25. The system as recited in claim 24, wherein the activating circuitry is tactilely initiated by a user of the telephone extension.

26. The system as recited in claim 25, wherein the voice signal originated from the call.

27. A telephone call and voice processing system comprising:

switching circuitry for receiving a call, wherein the switching circuitry connects the call to a telecommunications device coupled to the system, wherein two or more of the plurality of telecommunications devices each further comprises both a speaker and a microphone for enabling a user to audibly communicate with the call;

voice processing circuitry for automatically interacting with the call, wherein the switching circuitry and the voice processing circuitry are controlled by a single processing means;

circuitry for listening to a voice signal at a telephone extension coupled to the system;

circuitry for activating a recording sequence to record the voice signal; and

circuitry for storing the recorded voice signal in a digital memory, wherein the activating circuitry is tactically initiated by a user of the telephone extension, wherein the voice signal originated from a voice mail message stored in the system.

58. In a telephone call and voice processing system comprising switching circuitry for receiving an incoming call from a source external to the system, wherein the switching circuitry connects the incoming call to a telecommunications device coupled to the system from among a plurality of telecommunications devices connected as telephone extensions to the system, and voice processing circuitry for automatically interacting with the call, wherein the switching circuitry and the voice processing circuitry are controlled by a single processing means, a method comprising the steps of:

listening to a voice signal at a telephone extension coupled to the system;

activating a recording sequence to record the voice signal; and

storing the recorded voice signal in a memory.

59. The method as recited in claim 58, wherein the activating step is tactilely initiated by a user of the telephone extension.

60. The method as recited in claim 58, wherein the voice signal originated from the call to the system.

61. The method as recited in claim 58, wherein the voice signal originated from a voice mail message stored in the system.

69. A telephone call and voice processing system comprising:

switching circuitry for receiving an incoming call from a source external to the system, wherein the switching circuitry connects the incoming call to one of a plurality of telecommunications devices coupled to the system as extensions to the system; and

voice processing circuitry for automatically interacting with the call, wherein the switching circuitry and the voice processing circuitry are controlled by a single microprocessor.

70. A telephone call and voice processing system comprising:

switching circuitry for receiving a call, wherein the switching circuitry connects the call to one of a plurality of telecommunications devices coupled to the system; and

voice processing circuitry for automatically interacting with the call, wherein the switching circuitry further comprises a digital cross-point matrix.

71. A telephone call and voice processing system comprising:

switching circuitry for receiving a call, wherein the switching circuitry connects the call to one of a plurality of telecommunications devices coupled to the system;

the plurality of telecommunications devices connected to the system as telephone extensions accessible solely through the switching circuitry;

voice processing circuitry for automatically interacting with the call, wherein the switching circuitry and the voice processing circuitry are controlled by a single processing means;

circuitry for listening to a voice signal at one of the telephone extensions coupled to the system;

circuitry for activating a recording sequence to record the voice signal; and

circuitry for storing the recorded voice signal in a digital memory.

72. A telephone call and voice processing system comprising:

switching circuitry for receiving a call, wherein the switching circuitry connects the call to a telecommunications device coupled to the system;

voice processing circuitry for automatically interacting with the call, wherein the switching circuitry and the voice processing circuitry are controlled by a single processing means; and

circuitry for permitting a user of a telephone coupled to the system to monitor a voice mail message while the message is being recorded into the user's mailbox.

73. The system as recited in claim 1, wherein the information is detected DTMF tones.

74. The system as recited in claim 1, wherein the call is received by the switching circuitry from a central office trunk line.

75. The system as recited in claim 6, wherein the call is received from a source external to the system, and is connected to one of the telecommunications devices in accordance with detected DTMF tones accompanying the call, wherein the DTMF tones identify the telecommunications device to which the call is directed.

76. A telephone call and voice processing system comprising:

switching circuitry for receiving a call, wherein the switching circuitry connects the call to a telecommunications device coupled to the system; and

voice processing circuitry for automatically interacting with the call, wherein the switching circuitry and the voice processing circuitry are controlled by a single processing means, wherein the voice processing circuitry further comprises a signal processing circuitry coupled to the single processing means, wherein the signal processing circuitry further includes:

a DTMF receiver operable for recognizing DTMF tones from the call and instructing the switching circuitry to connect the call to the telecommunications device identified by the DTMF tones, wherein the telecommunications device is one of a plurality of telephone extensions connected to the switching circuitry.

77. A telephone call and voice processing system comprising:

switching circuitry for receiving a call, wherein the switching circuitry connects the call to a telecommunications device coupled to the system;

voice processing circuitry for automatically interacting with the call, wherein the switching circuitry and the voice processing circuitry are controlled by a single processing means;

circuitry for listening to a voice signal at a telephone extension coupled to the system;

circuitry for activating a recording sequence to record the voice signal; and

circuitry for storing the recorded voice signal in a digital memory, wherein the activating circuitry is tactically initiated by a user of the telephone extension, wherein the voice signal originated from a voice mail message stored in the system, wherein the call is an incoming call received by the switching circuitry via a central office trunk line, and wherein the switching circuitry connects the incoming call to one of a plurality of telecommunications devices coupled to the system as telephone extensions to the system.

78. The method as recited in claim 58, wherein the external source is a central office trunk line.

79. The method as recited in claim 58, wherein the switching circuitry connects the incoming call to one of the plurality of telecommunications devices in response to information accompanying the incoming call that identifies the telecommunications device to which the incoming call is connected to.

80. The system as recited in claim 69, wherein the external source is a central office trunk line.

81. The system as recited in claim 69, wherein the switching circuitry connects the incoming call to one of the plurality of extensions in response to information accompanying the incoming call that identifies the one of the plurality of extensions.

82. The system as recited in claim 81, wherein the information is detected DTMF tones.

83. A telephone call and voice processing system comprising:

a single microprocessor;

switching circuitry controlled by the single microprocessor;

a trunk line connected to the switching circuitry and adaptable for connecting to central office trunk circuitry;

a plurality of telephone extensions;

extension lines coupling the plurality of telephone extensions to the switching circuitry, wherein a call received by the switching circuitry over the trunk line is

connected to one of the plurality of telephone extensions by the switching circuitry in response to information accompanying the call which identifies the one of the plurality of telephone extensions the call desires to be connected to; and

voice processing circuitry for automatically interacting with the call such as for coupling the call to a voice mail box associated with the one of the telephone extensions.

84. The system as recited in claim 1, wherein each of the two or more of the plurality of telecommunications devices are separately operable telephone extensions.

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ZARLINK SEMICONDUCTOR

ISO-CMOS ST-BUS™ Family

MT8980D
Digital Switch

Data Sheet

February 2005

Features

- Zarlink ST-BUS compatible
- 8-line x 32-channel inputs
- 8-line x 32-channel outputs
- 256 ports non-blocking switch
- Single power supply (+5 V)
- Low power consumption: 30 mW Typ.
- Microprocessor-control interface
- Three-state serial outputs

Ordering Information

MT8980DE	40 Pin PDIP	Tubes
MT8980DP	44 Pin PLCC	Tubes
MT8980DPR	44 Pin PLCC	Tape & Reel
MT8980DP1	44 Pin PLCC*	Tubes
MT8980DE1	40 Pin PDIP*	Tubes
MT8980DPR1	44 Pin PLCC*	Tape & Reel

*Pb Free Matte Tin

-40°C to +85°C

Description

This VLSI ISO-CMOS device is designed for switching PCM-encoded voice or data, under microprocessor control, in a modern digital exchange, PBX or Central Office. It provides simultaneous connections for up to 256 64 kbit/s channels. Each of the eight serial inputs and outputs consist of 32 64 kbit/s channels multiplexed to form a 2048 kbit/s ST-BUS stream. In addition, the MT8980 provides microprocessor read and write access to individual ST-BUS channels.

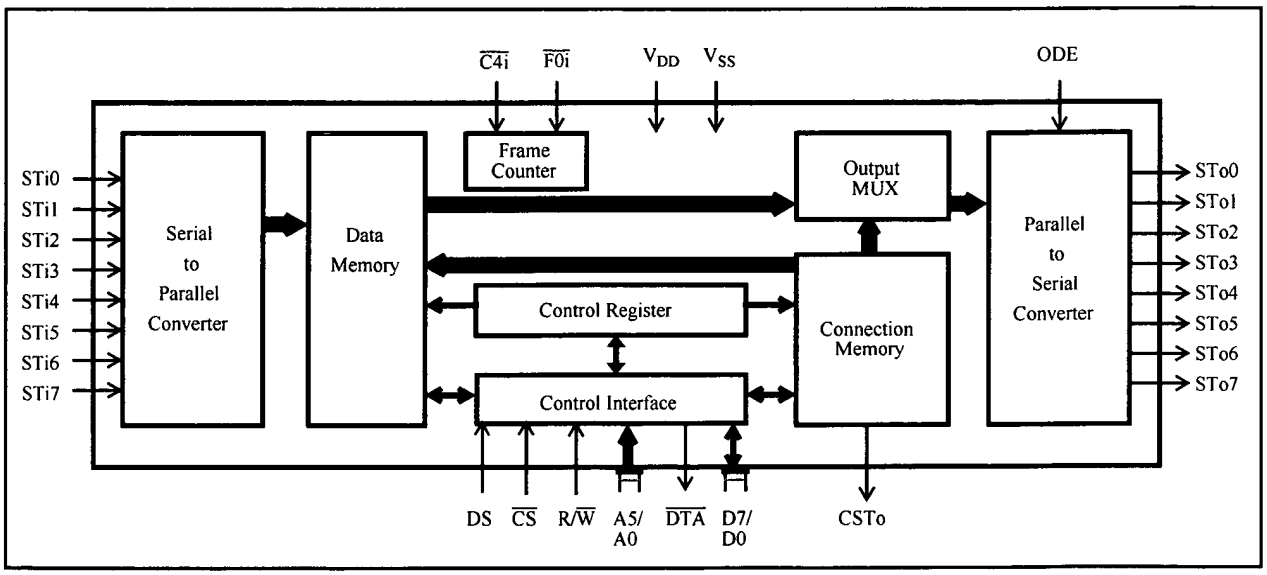


Figure 1 - Functional Block Diagram

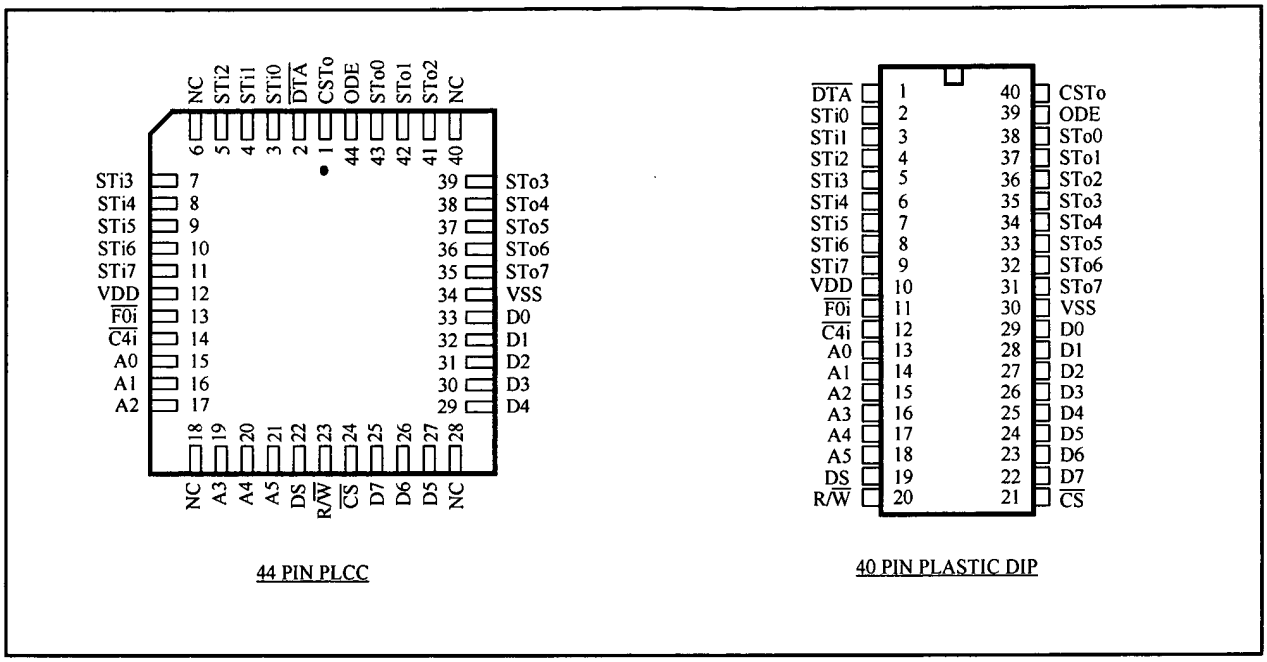


Figure 2 - Pin Connections

Pin Description

Pin #		Name	Description
40 DIP	44 PLCC		
1	2	$\overline{DTA}$	**Data Acknowledgement (Open Drain Output).** This is the data acknowledgement on the microprocessor interface. This pin is pulled low to signal that the chip has processed the data. A 909 Ω, 1/4W, resistor is recommended to be used as a pullup.
2-4	3-5	STi0-STi2	**ST-BUS Input 0 to 2 (Inputs).** These are the inputs for the 2048 kbit/s ST-BUS input streams.
5-9	7-11	STi3-STi7	**ST-BUS Input 3 to 7 (Inputs).** These are the inputs for the 2048 kbit/s ST-BUS input streams.
10	12	V_{DD}	**Power Input.** Positive Supply.
11	13	$\overline{F0i}$	**Framing 0-Type (Input).** This is the input for the frame synchronization pulse for the 2048 kbit/s ST-BUS streams. A low on this input causes the internal counter to reset on the next negative transition of $\overline{C4i}$.
12	14	$\overline{C4i}$	**4.096 MHz Clock (Input).** ST-BUS bit cell boundaries lie on the alternate falling edges of this clock.
13-15	15-17	A0-A2	**Address 0 to 2 (Inputs).** These are the inputs for the address lines on the microprocessor interface.
16-18	19-21	A3-A5	**Address 3 to 5 (Inputs).** These are the inputs for the address lines on the microprocessor interface.
19	22	DS	**Data Strobe (Input).** This is the input for the active high data strobe on the microprocessor interface.
20	23	R/$\overline{W}$	**Read or Write (Input).** This is the input for the read/write signal on the microprocessor interface - high for read, low for write.
21	24	$\overline{CS}$	**Chip Select (Input).** This is the input for the active low chip select on the microprocessor interface

Pin Description (continued)

Pin #		Name	Description
40 DIP	44 PLCC		
22-24	25-27	D7-D5	**Data 7 to 5 (Three-state I/O Pins).** These are the bidirectional data pins on the microprocessor interface.
25-29	29-33	D4-D0	**Data 4 to 0 (Three-state I/O Pins).** These are the bidirectional data pins on the microprocessor interface.
30	34	V_{SS}	**Power Input.** Negative Supply (Ground).
31-35	35-39	STo7-STo3	**ST-BUS Output 7 to 3 (Three-state Outputs).** These are the pins for the eight 2048 kbit/s ST-BUS output streams.
36-38	41-43	STo2-STo0	**ST-BUS Output 2 to 0 (Three-state Outputs).** These are the pins for the eight 2048 kbit/s ST-BUS output streams.
39	44	ODE	**Output Drive Enable (Input).** If this input is held high, the STo0-STo7 output drivers function normally. If this input is low, the STo0-STo7 output drivers go into their high impedance state. **NB:** Even when ODE is high, channels on the STo0-STo7 outputs can go high impedance under software control.
40	1	CSTo	**Control ST-BUS Output (Complementary Output).** Each frame of 256 bits on this ST-BUS output contains the values of bit 1 in the 256 locations of the Connection Memory High.
	6, 18, 28, 40	NC	No Connection.

Functional Description

In recent years, there has been a trend in telephony towards digital switching, particularly in association with software control. Simultaneously, there has been a trend in system architectures towards distributed processing or multi-processor systems.

In accordance with these trends, Zarlink has devised the ST-BUS (Serial Telecom Bus). This bus architecture can be used both in software-controlled digital voice and data switching, and for interprocessor communications. The uses in switching and in interprocessor communications are completely integrated to allow for a simple general purpose architecture appropriate for the systems of the future.

The serial streams of the ST-BUS operate continuously at 2048 kbit/s and are arranged in 125 µs wide frames which contain 32 8-bit channels. Zarlink manufactures a number of devices which interface to the ST-BUS; a key device being the MT8980 chip.

The MT8980 can switch data from channels on ST-BUS inputs to channels on ST-BUS outputs, and simultaneously allows its controlling microprocessor to read channels on ST-BUS inputs or write to channels on ST-BUS outputs (Message Mode). To the microprocessor, the MT8980 looks like a memory peripheral. The microprocessor can write to the MT8980 to establish switched connections between input ST-BUS channels and output ST-BUS channels, or to transmit messages on output ST-BUS channels. By reading from the MT8980, the microprocessor can receive messages from ST-BUS input channels or check which switched connections have already been established.

By integrating both switching and interprocessor communications, the MT8980 allows systems to use distributed processing and to switch voice or data in an ST-BUS architecture.

Hardware Description

Serial data at 2048 kbit/s is received at the eight ST-BUS inputs (STi0 to STi7), and serial data is transmitted at the eight ST-BUS outputs (STo0 to STo7). Each serial input accepts 32 channels of digital data, each channel containing an 8-bit word which may represent a PCM-encoded analog/voice sample as provided by a codec (e.g., Zarlink's MT8964).

This serial input word is converted into parallel data and stored in the 256 X 8 Data Memory. Locations in the Data Memory are associated with particular channels on particular ST-BUS input streams. These locations can be read by the microprocessor which controls the chip.

Locations in the Connection Memory, which is split into high and low parts, are associated with particular ST-BUS output streams. When a channel is due to be transmitted on an ST-BUS output, the data for the channel can either be switched from an ST-BUS input or it can originate from the microprocessor. If the data is switched from an input, then the contents of the Connection Memory Low location associated with the output channel is used to address the Data Memory. This Data Memory address corresponds to the channel on the input ST-BUS stream on which the data for switching arrived. If the data for the output channel originates from the microprocessor (Message Mode), then the contents of the Connection Memory Low location associated with the output channel are output directly, and this data is output repetitively on the channel once every frame until the microprocessor intervenes.

The Connection Memory data is received, via the Control Interface, at D7 to D0. The Control Interface also receives address information at A5 to A0 and handles the microprocessor control signals $\overline{CS}$, $\overline{DTA}$, R/$\overline{W}$ and DS. There are two parts to any address in the Data Memory or Connection Memory. The higher order bits come from the Control Register, which may be written to or read from via the Control Interface. The lower order bits come from the address lines directly.

The Control Register also allows the chip to broadcast messages on all ST-BUS outputs (i.e., to put every channel into Message Mode), or to split the memory so that reads are from the Data Memory and writes are to the Connection Memory Low. The Connection Memory High determines whether individual output channels are in Message Mode, and allows individual output channels to go into a high-impedance state, which enables arrays of MT8980s to be constructed. It also controls the CSTo pin.

All ST-BUS timing is derived from the two signals $\overline{C4i}$ and $\overline{F0i}$.

A5	A4	A3	A2	A1	A0	HEX ADDRESS	LOCATION
0	X	X	X	X	X	00 - 1F	Control Register *
1	0	0	0	0	0	20	Channel 0†
1	0	0	0	0	1	21	Channel 1†
•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•
1	1	1	1	1	1	3F	Channel 31†

* Writing to the Control Register is the only fast transaction.
† Memory and stream are specified by the contents of the Control Register.

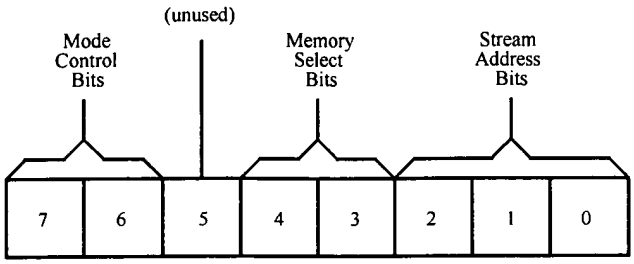
Figure 3 - Address Memory Map

Software Control

The address lines on the Control Interface give access to the Control Register directly or, depending on the contents of the Control Register, to the High or Low sections of the Connection Memory or to the Data Memory.

If address line A5 is low, then the Control Register is addressed regardless of the other address lines (see Fig. 3). If A5 is high, then the address lines A4-A0 select the memory location corresponding to channel 0-31 for the memory and stream selected in the Control Register.

The data in the Control Register consists of mode control bits, memory select bits, and stream address bits (see Fig. 4). The memory select bits allow the Connection Memory High or Low or the Data Memory to be chosen, and the stream address bits define one of the ST-BUS input or output streams.



BIT	NAME	DESCRIPTION
7	**Split Memory**	When 1, all subsequent reads are from the Data Memory and writes are to the Connection Memory Low, except when the Control Register is accessed again. When 0, the Memory Select bits specify the memory for subsequent operations. In either case, the Stream Address Bits select the subsection of the memory which is made available.
6	**Message Mode**	When 1, the contents of the Connection Memory Low are output on the Serial Output streams except when the ODE pin is low. When 0, the Connection Memory bits for each channel determine what is output.
5	**(unused)**	
4-3	**Memory Select Bits**	0-0 - Not to be used 0-1 - Data Memory (read only from the microprocessor port) 1-0 - Connection Memory Low 1-1 - Connection Memory High
2-0	**Stream Address Bits**	The number expressed in binary notation on these bits refers to the input or output ST-BUS stream which corresponds to the subsection of memory made accessible for subsequent operations.

Figure 4 - Control Register Bits

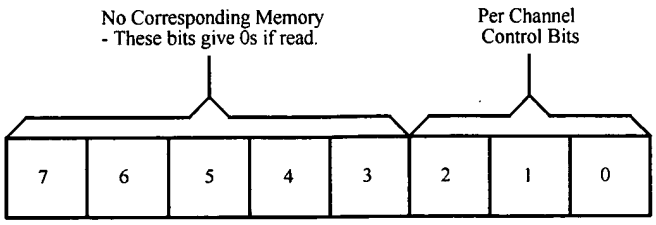
Bit 7 of the Control Register allows split memory operation - reads are from the Data Memory and writes are to the Connection Memory Low.

The other mode control bit, bit 6, puts every output channel on every output stream into active Message Mode; i.e., the contents of the Connection Memory Low are output on the ST-BUS output streams once every frame unless the ODE pin is low. In this mode the chip behaves as if bits 2 and 0 of every Connection Memory High location were 1, regardless of the actual values.

If bit 6 of the Control Register is 0, then bits 2 and 0 of each Connection Memory High location function normally (see Fig. 5). If bit 2 is 1, the associated ST-BUS output channel is in Message Mode; i.e., the byte in the corresponding Connection Memory Low location is transmitted on the stream at that channel. Otherwise, one of the bytes received on the serial inputs is transmitted and the contents of the Connection Memory Low define the ST-BUS input stream and channel where the byte is to be found (see Fig. 6).

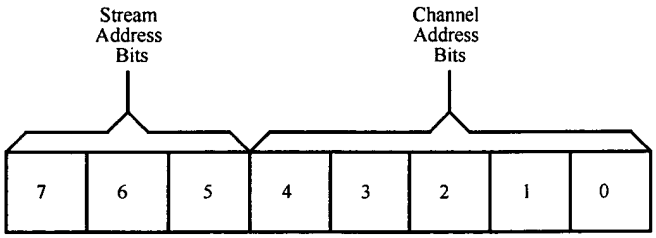
If the ODE pin is low, then all serial outputs are high-impedance. If it is high and bit 6 in the Control Register is 1, then all outputs are active. If the ODE pin is high and bit 6 in the Control Register is 0, then the bit 0 in the Connection Memory High location enables the output drivers for the corresponding individual ST-BUS output stream and channel. Bit 0=1 enables the driver and bit 0=0 disables it (see Fig. 5).

Bit 1 of each Connection Memory High location (see Fig. 5) is output on the CSTo pin once every frame. To allow for delay in any external control circuitry the bit is output one channel before the corresponding channel on the ST-BUS streams, and the bit for stream 0 is output first in the channel; e.g., bit 1's for channel 9 of streams 0-7 are output synchronously with ST-BUS channel 8 bits 7-0.



BIT	NAME	DESCRIPTION
2	**Message Channel**	When 1, the contents of the corresponding location in Connection Memory Low are output on the location's channel and stream. When 0, the contents of the corresponding location in Connection Memory Low act as an address for the Data Memory and so determine the source of the connection to the location's channel and stream.
1	**CSTo Bit**	This bit is output on the CSTo pin one channel early. The CSTo bit for stream 0 is output first.
0	**Output Enable**	If the ODE pin is high and bit 6 of the Control Register is 0, then this bit enables the output driver for the location's channel and stream. This allows individual channels on individual streams to be made high-impedance, allowing switching matrices to be constructed. A 1 enables the driver and a 0 disables it.

Figure 5 - Connection Memory High Bits



BIT	NAME	DESCRIPTION
7-5*	**Stream Address Bits***	The number expressed in binary notation on these 3 bits is the number of the ST-BUS stream for the source of the connection. Bit 7 is the most significant bit. e.g., if bit 7 is 1, bit 6 is 0 and bit 5 is 0, then the source of the connection is a channel on STi4.
4-0*	**Channel Address Bits***	The number expressed in binary notation on these 5 bits is the number of the channel which is the source of the connection (The ST-BUS stream where the channel lies is defined by bits 7, 6 and 5.). Bit 4 is the most significant bit. e.g., if bit 4 is 1, bit 3 is 0, bit 2 is 0, bit 1 is 1 and bit 0 is 1, then the source of the connection is channel 19.

*If bit 2 of the corresponding Connection High location is 1 or if bit 6 of the Control Register is 1, then these entire 8 bits are output on the channel and stream associated with this location. Otherwise, the bits are used as indicated to define the source of the connection which is output on the channel and stream associated with this location.

Figure 6 - Connection Memory Low Bits

Applications

Use in a Simple Digital Switching System

Figs. 7 and 8 show how MT8980s can be used with MT8964s to form a simple digital switching system. Fig. 7 shows the interface between the MT8980s and the filter/codecs. Fig. 8 shows the position of these components in an example architecture.

The MT8964 filter/codec in Fig. 7 receives and transmits digitized voice signals on the ST-BUS input D_R, and ST-BUS output D_X, respectively. These signals are routed to the ST-BUS inputs and outputs on the top MT8980, which is used as a digital speech switch.

The MT8964 is controlled by the ST-BUS input D_C originating from the bottom MT8980, which generates the appropriate signals from an output channel in Message Mode. This architecture optimizes the messaging capability of the line circuit by building signalling logic, e.g., for on-off hook detection, which communicates on an ST-BUS output. This signalling ST-BUS output is monitored by a microprocessor (not shown) through an ST-BUS input on the bottom MT8980.

Fig. 8 shows how a simple digital switching system may be designed using the ST-BUS architecture. This is a private telephone network with 256 extensions which uses a single MT8980 as a speech switch and a second MT8980 for communication with the line interface circuits.

A larger digital switching system may be designed by cascading a number of MT8980s. Fig. 9 shows how four MT8980s may be arranged in a non-blocking configuration which can switch any channel on any of the ST-BUS inputs to any channel on the ST-BUS outputs.

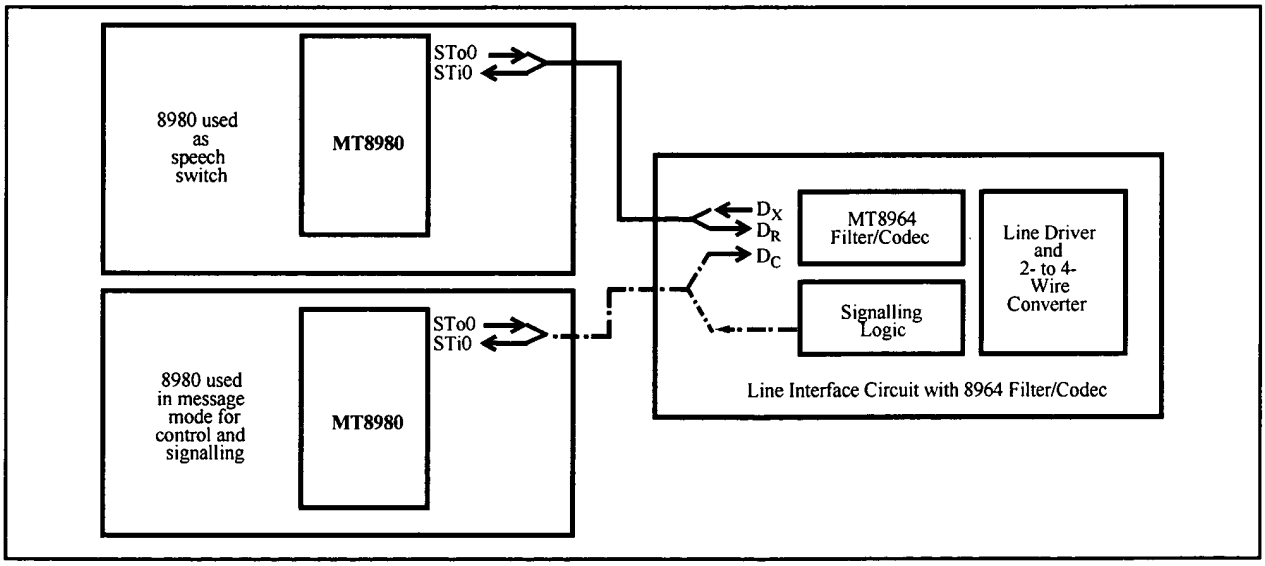


Figure 7 - Example of Typical Interface between 8980s and 8964s for Simple Digital Switching System

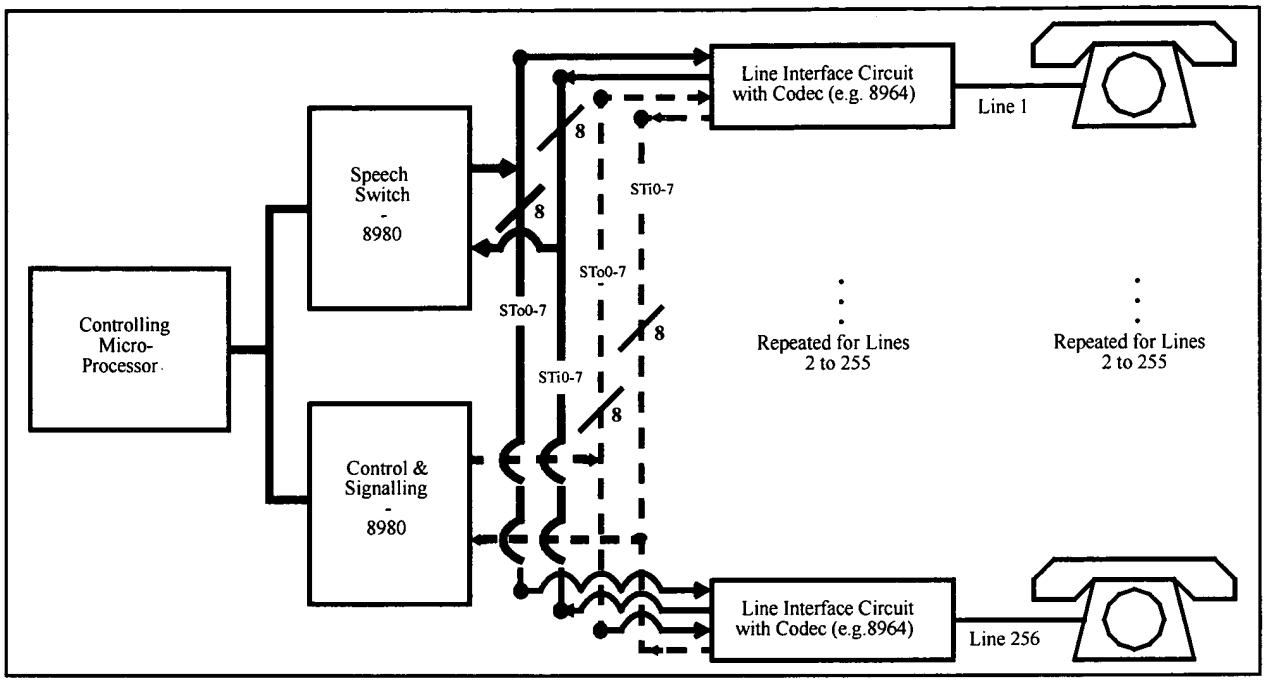


Figure 8 - Example Architecture of a Simple Digital Switching System

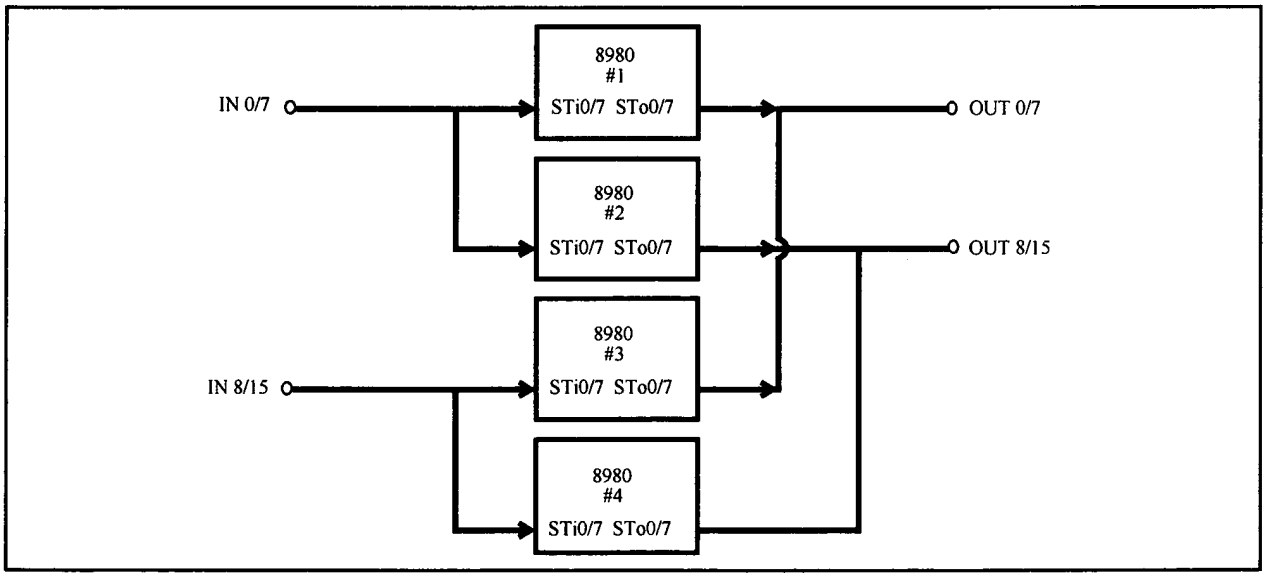


Figure 9 - Four 8980s Arranged in a Non-Blocking 16 x 16 Configuration

Application Circuit with 6802 Processor

Fig. 10 shows an example of a complete circuit which may be used to evaluate the chip.

For convenience, a 4 MHz crystal oscillator has been used rather than a 4.096 MHz clock, as both are within the limits of the chip's specifications. The RC delay used with the 393 counters ensures a sufficient hold time for the $\overline{FP}$ signal, but the values used may have to be changed if faster 393 counters become available.

The chip is shown as memory mapped into the MEK6802D3 system. Chip addresses 00-3F correspond to processor addresses 2000-203F. Delay through the address decoder requires the VMA signal to be used twice to remove glitches. The MEK6802D3 board uses a 10 KΩ pullup on the MR pin, which would have to be incorporated into the circuit if the board was replaced by a processor.

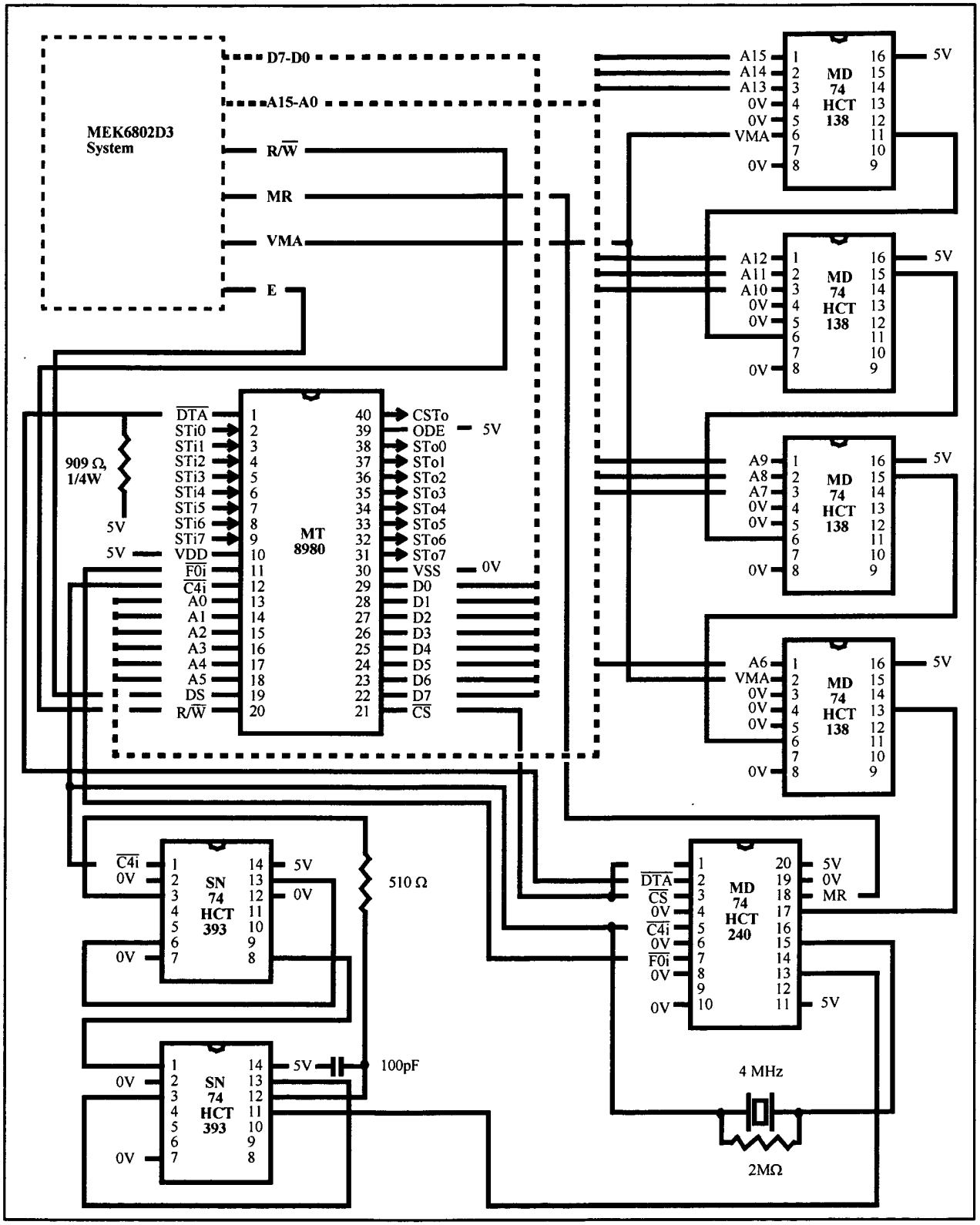


Figure 10 - Application Circuit with 6802

Absolute Maximum Ratings*

	Parameter	Symbol	Min.	Max.	Units
1	V_{DD} - V_{SS}		-0.3	7	V
2	Voltage on Digital Inputs	V_I	V_{SS}-0.3	V_{DD}+0.3	V
3	Voltage on Digital Outputs	V_O	V_{SS}-0.3	V_{DD}+0.3	V
4	Current at Digital Outputs	I_O		40	mA
5	Storage Temperature	T_S	-65	+150	°C
6	Package Power Dissipation	P_D		2	W

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Operating Temperature	T_{OP}	-40		+85	°C	
2	Positive Supply	V_{DD}	4.75		5.25	V	
3	Input Voltage	V_I	0		V_{DD}	V	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

		Characteristics	Sym.	Min.	Typ.‡			
1	INPUTS	Supply Current	I_{DD}		6	10	mA	Outputs unloaded
2		Input High Voltage	V_{IH}	2.0			V	
3		Input Low Voltage	V_{IL}			0.8	V	
4		Input Leakage	I_{IL}			5	µA	V_I between V_{SS} and V_{DD}
5		Input Pin Capacitance	C_I		8		pF	
6	OUTPUTS	Output High Voltage	V_{OH}	2.4			V	I_{OH} = 10 mA
7		Output High Current	I_{OH}	10	15		mA	Sourcing. V_{OH}=2.4V
8		Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 5 mA
9		Output Low Current	I_{OL}	5	10		mA	Sinking. V_{OL} = 0.4V
10		High Impedance Leakage	I_{OZ}			5	µA	V_O between V_{SS} and V_{DD}
11		Output Pin Capacitance	C_O		8		pF	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

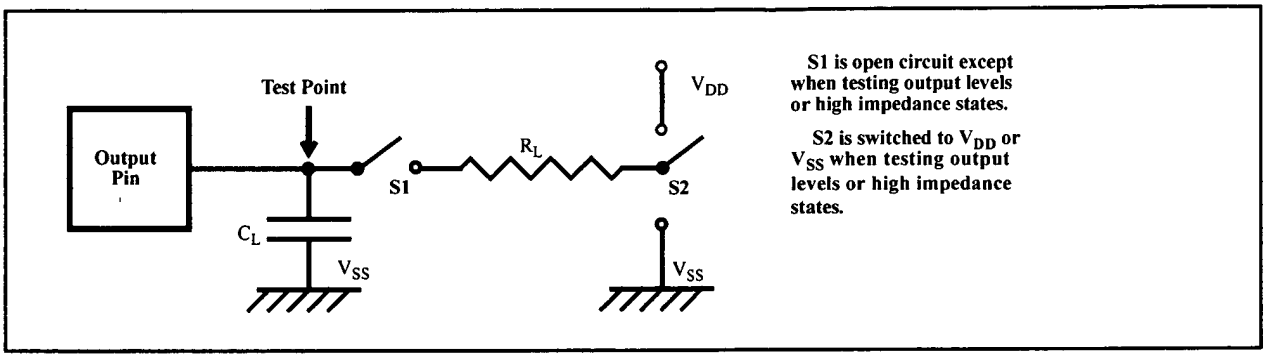


Figure 11 - Output Test Load

AC Electrical Characteristics† - Clock Timing (Figures 12 and 13)

		Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1		Clock Period*	t_{CLK}	220	244	300	ns	
2	I	Clock Width High	t_{CH}	95	122	150	ns	
3	N	Clock Width Low	t_{CL}	110	122	150	ns	
4	P	Clock Transition Time	t_{CTT}		20		ns	
5	U	Frame Pulse SetupTime	t_{FPS}	20		200	ns	
6	T	Frame Pulse Hold Time	t_{FPH}	0.020		50	µs	
7	S	Frame Pulse Width	t_{FPW}		244		ns	

† Timing is over recommended temperature & power supply voltages.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.
* Contents of Connection Memory are not lost if the clock stops, however, ST-BUS outputs go into the high impedance state.
NB: Frame Pulse is repeated every 512 cycles of $\overline{C4i}$.

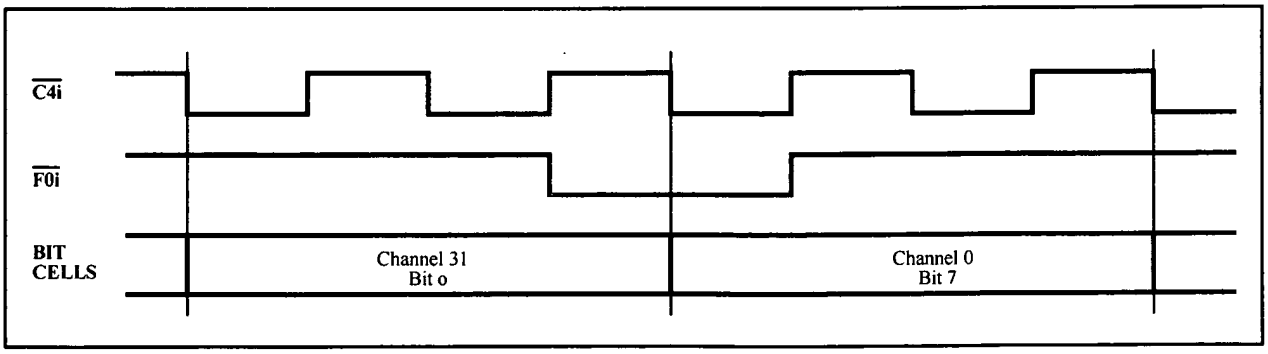


Figure 12 - Frame Alignment

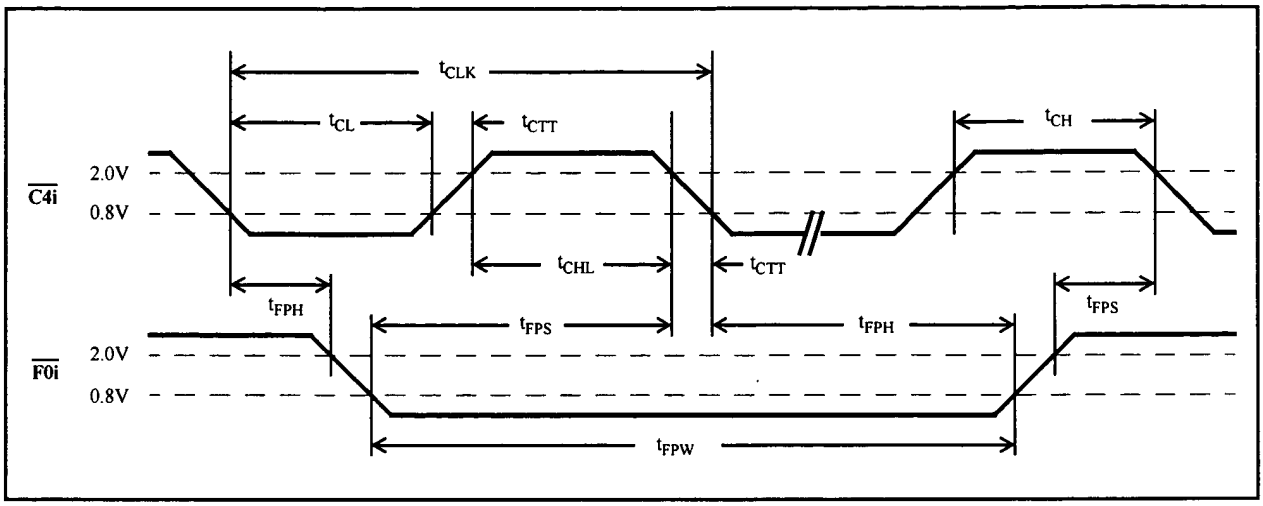


Figure 13 - Clock Timing

AC Electrical Characteristics† - Serial Streams (Figures 11, 14, 15 and 16)

		Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	OUTPUTS	STo0/7 Delay - Active to High Z	t_{SAZ}	20	50	80	ns	R_L=1 KΩ*, C_L=150 pF
2		STo0/7 Delay - High Z to Active	t_{SZA}	25	60	125	ns	C_L=150 pF
3		STo0/7 Delay - Active to Active	t_{SAA}	30	65	125	ns	C_L=150 pF
4		STo0/7 Hold Time	t_{SOH}	25	45		ns	C_L=150 pF
5		Output Driver Enable Delay	t_{OED}		45	125	ns	R_L=1 KΩ*, C_L=150 pF
6		External Control Hold Time	t_{XCH}	0	50		ns	C_L=150 pF
7		External Control Delay	t_{XCD}		75	110	ns	C_L=150 pF
8	IN	Serial Input Setup Time	t_{SIS}		-40	-20	ns	
9		Serial Input Hold Time	t_{SIH}	90			ns	

† Timing is over recommended temperature & power supply voltages.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.
* High Impedance is measured by pulling to the appropriate rail with R_L, with timing corrected to cancel time taken to discharge C_L.

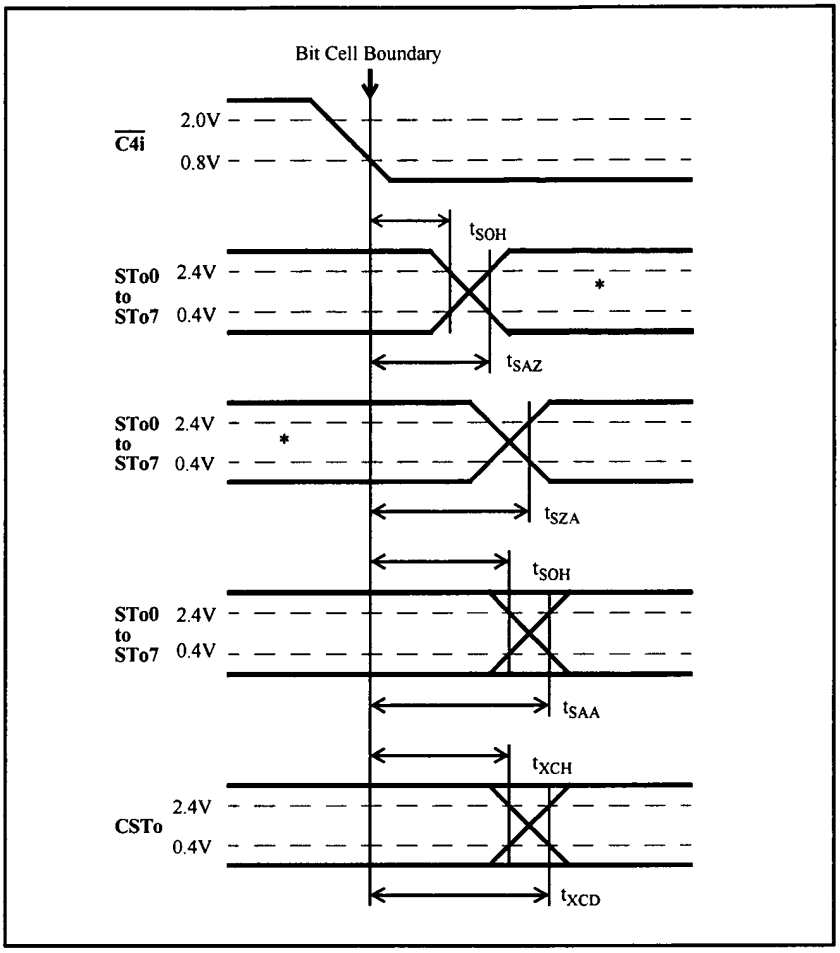


Figure 14 - Serial Outputs and External Control

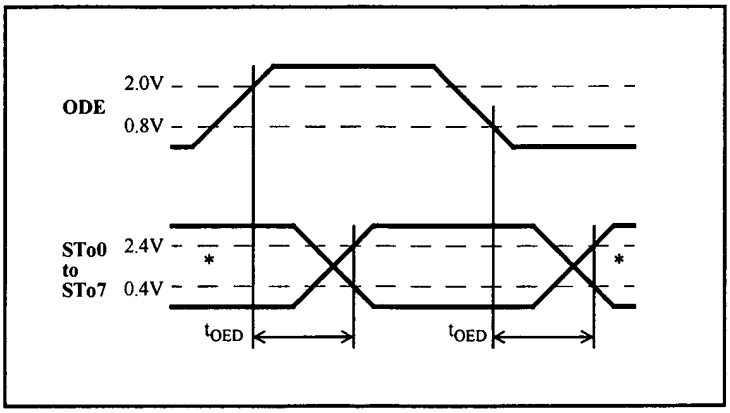


Figure 15 - Output Driver Enable

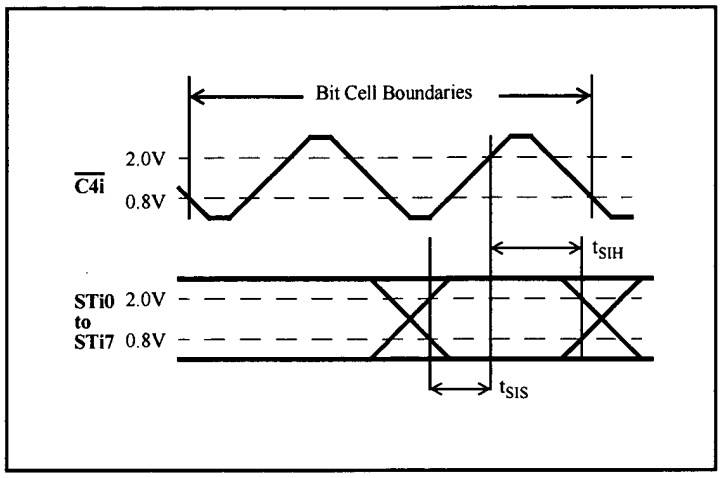


Figure 16 - Serial Inputs

AC Electrical Characteristics† - Processor Bus (Figures 11 and 17)

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Chip Select Setup Time	t_{CSS}	20	0		ns	
2	Read/Write Setup Time	t_{RWS}	25	5		ns	
3	Address Setup Time	t_{ADS}	25	5		ns	
4	Acknowledgement Delay Fast	t_{AKD}		40	100	ns	C_L=150 pF
	Slow	t_{AKD}	2.7		7.2	cycles	$\overline{C4i}$ cycles[1]
5	Fast Write Data Setup Time	t_{FWS}	20			ns	
6	Slow Write Data Delay	t_{SWD}		2.0	1.7	cycles	$\overline{C4i}$ cycles[1]
7	Read Data Setup Time	t_{RDS}			0.5	cycles	$\overline{C4i}$ cycles[1], C_L= 150 pF
8	Data Hold Time Read	t_{DHT}	20			ns	R_L=1 KΩ*, C_L=150 pF
	Write	t_{DHT}	20	10		ns	
9	Read Data To High Impedance	t_{RDZ}		50	90	ns	R_L=1 KΩ*, C_L=150 pF
10	Chip Select Hold Time	t_{CSH}	0			ns	
11	Read/Write Hold Time	t_{RWH}	0			ns	
12	Address Hold Time	t_{ADH}	0			ns	
13	Acknowledgement Hold Time	t_{AKH}	10	60	80	ns	R_L=1 KΩ*, C_L=150 pF

† Timing is over recommended temperature & power supply voltages.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.
* High Impedance is measured by pulling to the appropriate rail with R_L, with timing corrected to cancel time taken to discharge C_L.
1. Processor accesses are dependent on the $\overline{C4i}$ clock, and so some timings are expressed as multiples of the $\overline{C4i}$ clock period.

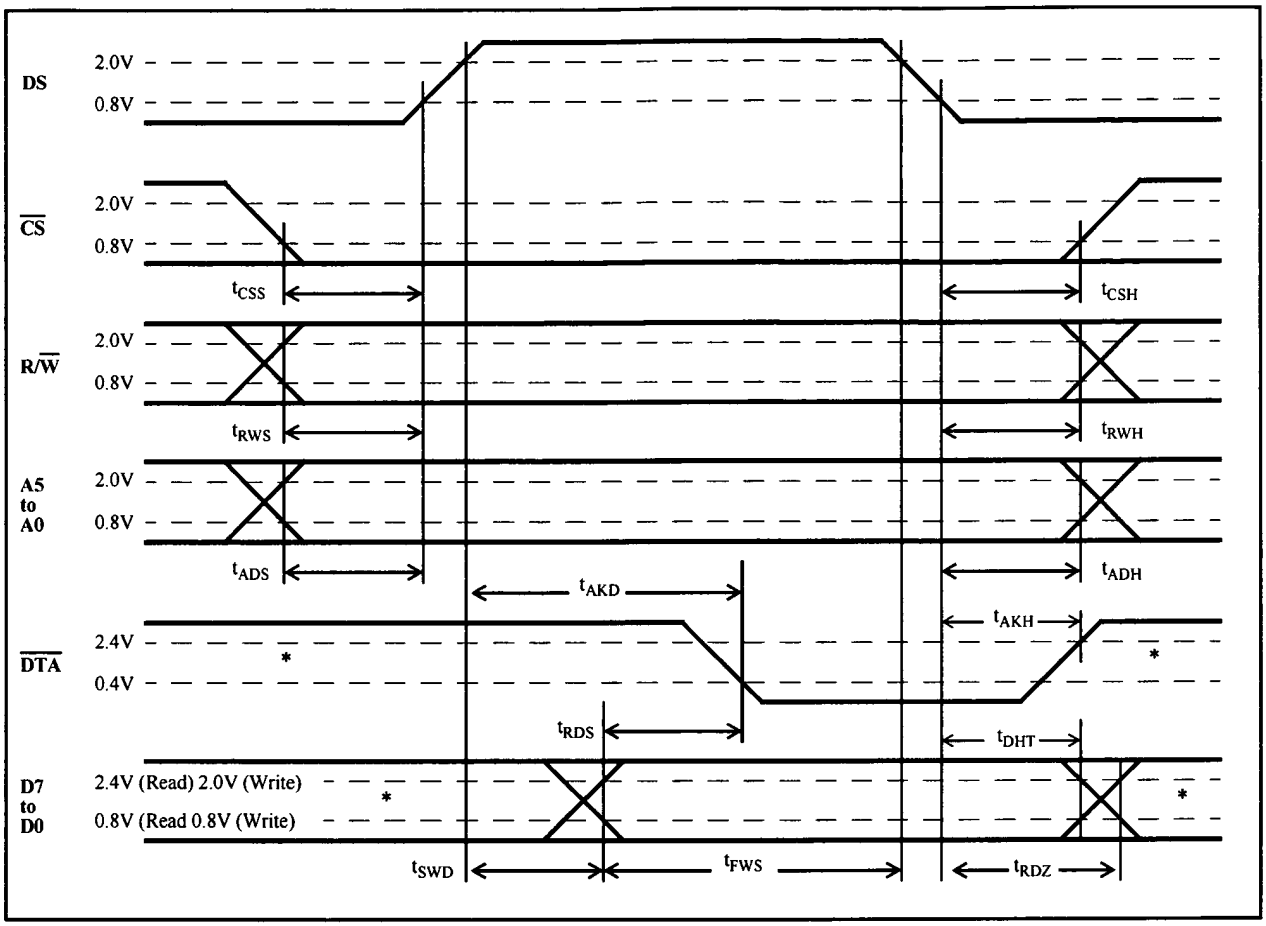
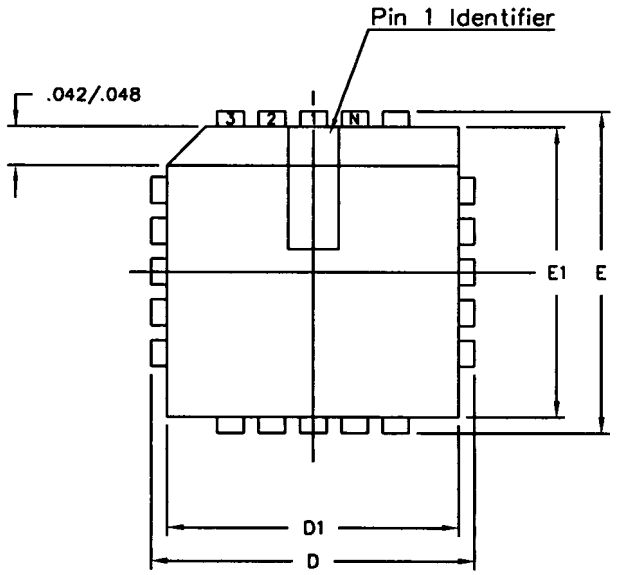
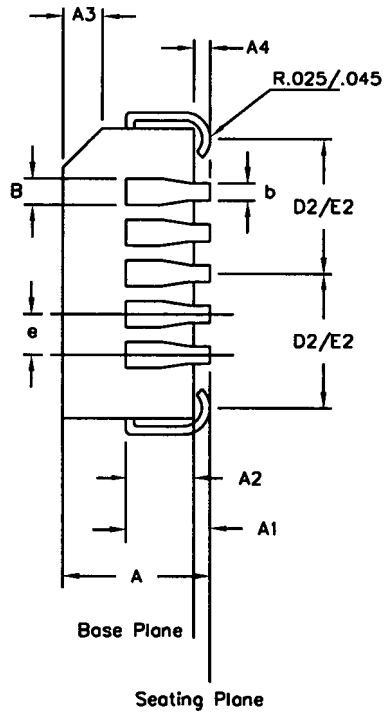


Figure 17 - Processor Bus





Symbol	Control Dimensions in inches		Altern. Dimensions in millimetres	
	MIN	MAX	MIN	MAX
A	0.165	0.180	4.19	4.57
A1	0.090	0.120	2.29	3.05
A2	0.062	0.083	1.57	2.11
A3	0.042	0.056	1.07	1.42
A4	0.020	–	0.51	–
D	0.685	0.695	17.40	17.65
D1	0.650	0.656	16.51	16.66
D2	0.291	0.319	7.39	8.10
E	0.685	0.695	17.40	17.65
E1	0.650	0.656	16.51	16.66
E2	0.291	0.319	7.39	8.10
B	0.026	0.032	0.66	0.81
b	0.013	0.021	0.33	0.53
e	0.050 BSC		1.27 BSC	
	Pin features			
ND	11			
NE	11			
N	44			
Note	Square			
Conforms to JEDEC MS-018AC Iss. A				

Notes:
1. All dimensions and tolerances conform to ANSI Y14.5M–1982
2. Dimensions D1 and E1 do not include mould protrusions. Allowable mould protrusion is 0.010" per side. Dimensions D1 and E1 include mould protrusion mismatch and are determined at the parting line, that is D1 and E1 are measured at the extreme material condition at the upper or lower parting line.
3. Controlling dimensions in Inches.
4. "N" is the number of terminals.
5. Not To Scale
6. Dimension R required for 120° minimum bend.

ISSUE	1	2	3	
ACN	5958	207470	213094	
DATE	15Aug94	10Sep99	15Jul02	
APPRD.				

ZARLINK SEMICONDUCTOR

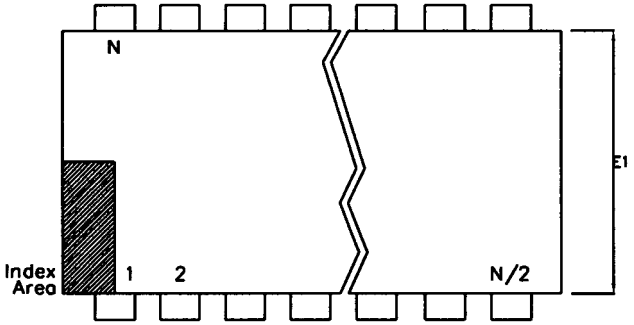
Previous package codes

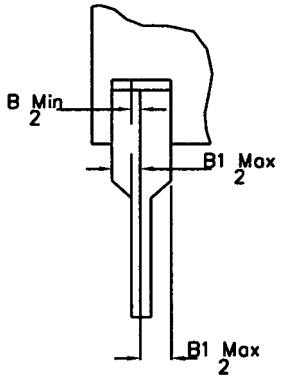
HP / P

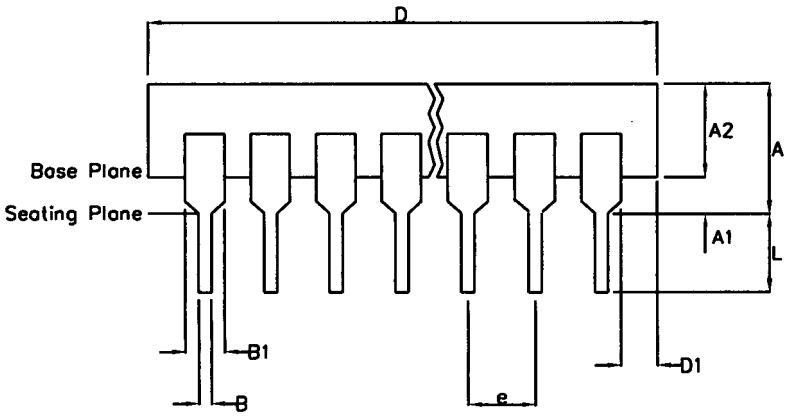
Package Code QA

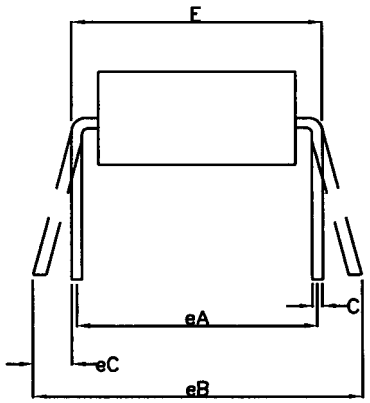
Package Outline for 44 lead PLCC

GPD00003









	Min mm	Max mm	Min Inches	Max Inches
A		6.35		0.250
A1	0.38		0.015	
A2	3.18	4.95	0.125	0.195
B	0.36	0.56	0.014	0.022
B1	0.76	1.78	0.030	0.070
C	0.20	0.38	0.008	0.015
D	50.29	53.21	1.980	2.095
D1	0.13		0.005	
E	15.24	15.88	0.600	0.625
E1	12.32	14.73	0.485	0.580
e	2.54 BSC		0.100 BSC	
eA	15.24 BSC		0.600 BSC	
eB		17.78		0.700
L	2.92	5.08	0.115	0.200
N	40		40	
Conforms to Jedec MS-011AC ISS.B				

Notes:
1. Controlling Dimensions are in inches
2. Dimension A, A1 and L are measured with the package seated in the Seating Plane
3. Dimensions D & E1 do not include mould flash or protrusions. Mould flash or protrusion shall not exceed 0.010 inch.
4. Dimensions E & eA are measured with leads constrained to be perpendicular to plane T.
5. Dimensions eB & eC are measured at the lead tips with the leads unconstrained; eC must be zero or greater.

ISSUE	1	2	3	
ACN	7010	203533	213103	
DATE	20Apr95	25Nov97	15Jul02	
APPRD.				

ZARLINK SEMICONDUCTOR

Previous package codes

DP / E

Package Code DA

Package Outline for 40 lead PDIP

GPD00073

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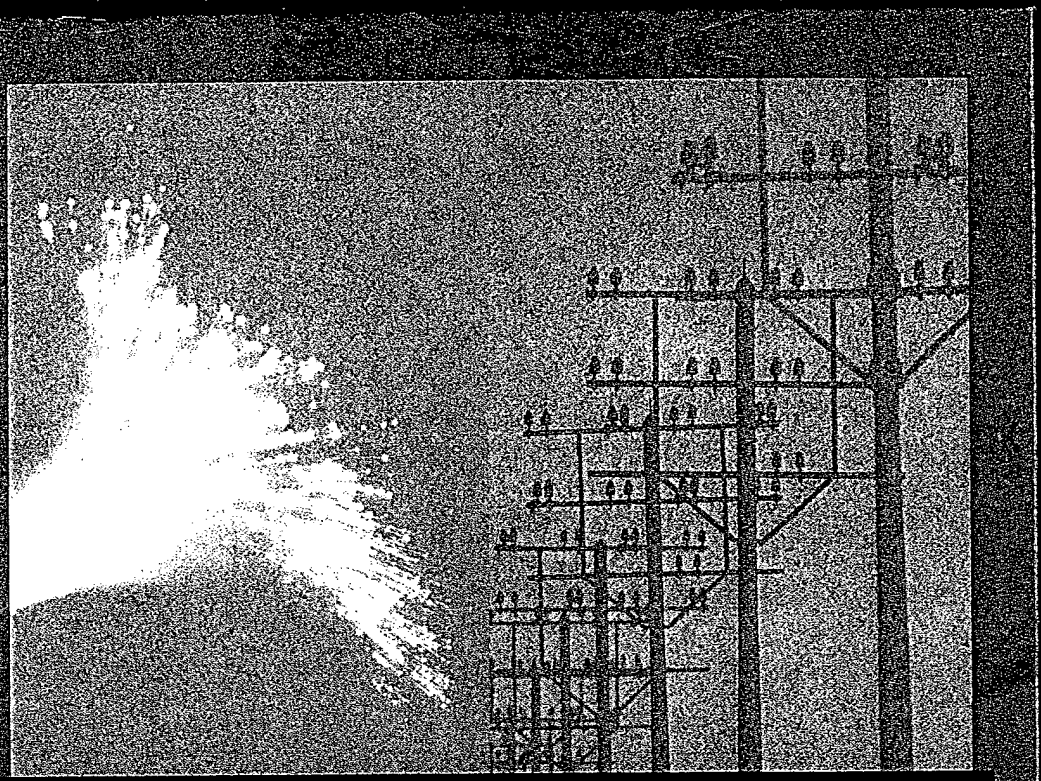

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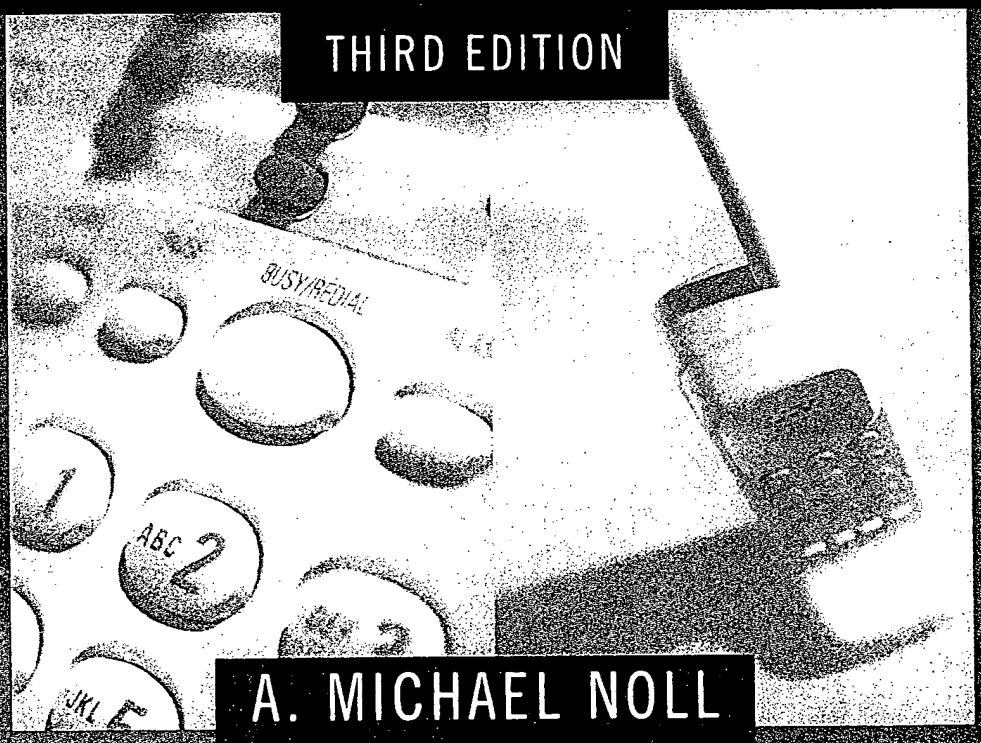
THIRD EDITION



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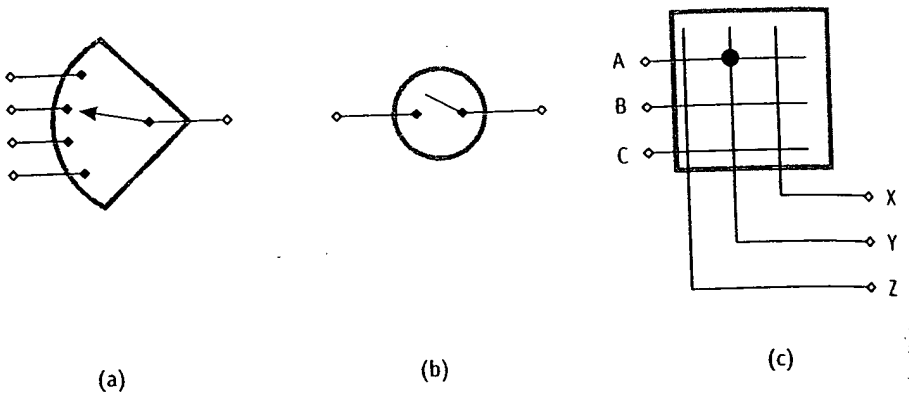

Figure 6.12 The basic types of switches used in space-division switching are (a) the rotary switch, (b) the on-off switch, and (c) the matrix switch.

is that electrical contacts must slide across each other, thereby subjecting them to considerable wear—and wear creates noise. Furthermore, the relatively large amount of mechanical motion means that a fair amount of time is needed to make an actual connection.

We are all familiar with the on-off switch that turns lamps on or off. In its electromechanical form, it consists only of two contacts and a means to complete or to open the circuit between them. Though simple, the electromechanical on-off switch is still subject to some wear, and though faster than a rotary switch, it is very slow in today's world of electronics. A transistor can be used as an on-off switch and offers the advantages of speed, low noise, and no wear.

On-off switches are used to create a basic coordinate, or matrix, switch. A matrix switch can connect many lines with many other lines. Connections are made with on-off switches at the crosspoints in a matrix of all input lines and all output lines. The electrical connection at each crosspoint can be made using a variety of electromechanical and electronic technologies, such as conventional contacts, small reed contacts sealed in glass, and diodes and transistors.

Switching stages

Normally, not everyone will want to converse with everyone else at the same time. Hence, a switching network does not need to be designed fo

interconnect between all
lines can therefore be c
number of switching path
switching, as shown in F
accomplished in stages c
expansion.

A basic three-stage swi
in Figure 6.14. The electr
connect one line to any on
used in the switching netw
step-by-step system is exp

A basic three-stage swit
in Figure 6.15. The electr
that can connect 10 inputs t
Bell Labs, is used in the swi
The crossbar system is exp

Many telephone calls a
office. To handle these cal
connected back on itself tc
connections. The lines usec
trunks.

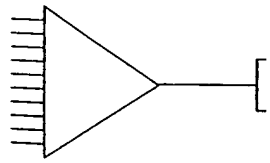

Figure 6.13 There are three
network. Many input lines are
serving lines. The ratio of the
than 1. These serving lines are
service to a large number of ou
lines to input serving lines is